REMARKS

This amendment is in response to the Office Action of April 14, 2003. Claims 1 through 3 are currently pending in the application. Claim 1 has been amended.

Applicant notes the filing of an Information Disclosure Statement herein on August 30, 2001 and notes that a copy of the PTO-1449 was not returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449 (which is the same as that of record to that date in the parent application hereto) be made of record herein.

Claims 1 through 3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ueda et al. (U.S. Patent 5,334,872) in combination with Golwalkar et al. (U.S. Patent 5,527,740). Reconsideration of the application is respectfully requested in light of the remarks presented herein.

Applicant submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Ueda teaches or suggests a packaged semiconductor device with a die pad 25 supported on an outer frame through hanging leads 26. The die pad 25 is suspended by the hanging leads 26. (See Col. 4, lines14-16 and Fig. 3)

Golwalkar teaches or suggests a method for constructing a dual-sided chip package on a lead frame having a die pad and lead fingers. A pair of clamping blocks are employed to *clamp the die pad.* (Col. 5 lines 61-62, emphasis added)

Claim 1, as amended herein, recites an assembly method for a semiconductor device assembly including forming a strip of lead frames having at least one integral clamping tab and

aligning said strip of lead frames having an upper clamp member overlying portions of the at least one integral clamping tab.

Neither Ueda nor Golwalkar nor any combination of Ueda and Golwalkar teach or suggest an upper clamp member overlying portions of an integral clamping tab as set forth in presently amended independent claim 1 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103regarding the claimed invention. Rather, Golwalkar teaches clamping blocks which clamp the die pad and Ueda fails to teach or suggest an upper clamp or an integral clamping tab. Therefore, the combination of Ueda and Golwakar cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention

Additionally, there is no suggestion or motivation to combine the reference teachings. The die pad 25 of Ueda is supported on an outer frame through hanging leads 26 as shown in Fig 3. Because the die pad is supported, there is no motivation to clamp the die pad with clamping blocks as taught by Golwalkar.

Accordingly, it is respectfully submitted that presently amended independent claim 1 is allowable.

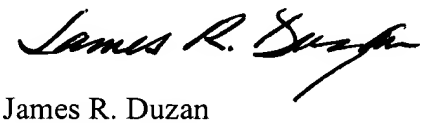
Claims 2 and 3 are each allowable, among other reasons, as depending from claim 1, which is allowable. Any claim depending on an independent claim which is nonobvious under 35 U.S.C. 103 is also nonobvious. *In re Fine,* 837 F.2d 1071 (Fed. Cir. 1988).

CONCLUSION

For the reasons set forth hereinabove, Applicant submits that claims 1 through 3 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1 through 3 and the case passed for issue.

Respectfully submitted,



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IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An assembly method for a semiconductor device assembly using a wire bonding device having an upper clamp member and a lower clamp member, said method comprising:

forming a strip of lead frames, said strip having opposed rails, having dam bars between said opposed rails, having at least two inner leads, having at least two outer leads, having a die mount paddle and having at least one integral clamping tab, said at least one integral clamping tab extending outwardly for contact by said upper clamp member;

attaching a semiconductor device to said die mount paddle, said semiconductor device having a plurality of bond pads;

aligning said strip of lead frames on said lower clamp member of said wire bonding device having said upper clamp member overlying portions of said at least two inner leads and portions of ~~said at least two outer leads of~~ said at least one integral clamping tab; and

attaching at least two bond wires to said plurality of bond pads of said semiconductor device and said portions of said at least two inner leads.

2. (Previously Amended) The method of claim 1, further comprising:

forming said die mount paddle having an upper surface thereof at a level below an upper level of said at least two inner leads; and

deforming said at least one integral clamping tab to clamp portions thereof.

3. (Previously Amended) The method of claim 1, further comprising:

removing said strip of lead frames and said semiconductor device from said lower clamp member; and

encapsulating a portion of said strip of lead frames, said semiconductor device, and said at least two bond wires extending between said strip of lead frames and said semiconductor device in a material.